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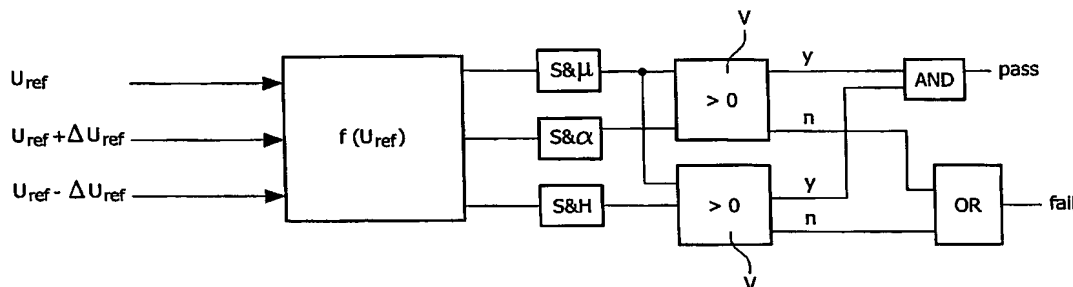
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(54) Title: METHOD AND CIRCUIT ARRANGEMENT FOR THE SELF-TESTING OF A REFERENCE VOLTAGE IN ELECTRONIC COMPONENTS



(57) Abstract: To provide a method for the self-testing of a reference voltage in electronic components, by means of which method there is defined a circuit arrangement for a self-test of the reference voltage that can be implemented in the form of an on-chip test, i.e. for which no external reference-voltage source is required, provision is made for the reference voltage (U_{ref}) to be the variable of a function $f(U_{ref})$ that has an extreme at the point where the selected nominal value ($U_{ref, test}$) of the reference voltage (U_{ref}) is situated and, in a self-test, for the values of the function to be determined in succession for the reference voltage (U_{ref}) and for two further test voltages ($U_{ref} + \Delta U_{ref}$, $U_{ref} - \Delta U_{ref}$) that differ from the reference voltage (U_{ref}) by only small positive and negative amounts ($+\Delta U_{ref}$, $-\Delta U_{ref}$) respectively and for these values to be compared with one another and, if the values of the function for the test voltages ($U_{ref} + \Delta U_{ref}$, $U_{ref} - \Delta U_{ref}$) differ from the value of the function for the reference voltage (U_{ref}) in the same direction, for a pass signal to be generated, or if not, for a fail signal to be generated.



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